AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 5 beginning with "Referring to Figure 1..." with the following paragraph:

Referring to Figure 1, a circuit diagram of the currently preferred embodiment of the present invention is shown. The circuit comprises a charge pump 101. Alternatively, a voltage multiplication circuit may be implemented in place of the charge pump 101. The charge pump 101 is typically comprised of a series of MOS diode connected transistors and coupling capacitors driven by two-phase non-overlapping clocks generated from a primary clock signal ~~labeled~~ OSC. The OSC signal is usually the output of an on-chip ring oscillator circuit 150. The OSC signal is also input to the divide by N counter 102. The divide by N counter 102 is a binary digital counter that performs a "divide by N" function where N is a power of two. The output from the divide by N counter 102 is a clock signal, OSCD, whose frequency is equal to that OSC divided by N where $N=2^M$, with being the width ~~of~~ in bits of the binary counter represented by the counter. The OSCD output from the divide by N counter 102 is fed as an input to the non-overlapping two-phase clock generator 103. The clock generator 103 generates two non-overlapping clock phases, PHI1 and PHI2, which have the same frequency as the output from the counter 102. The two non-overlapping clock phase signals are input to block 104. Block 104 creates two "gated" versions of the PHI1 and PHI2 signals, referred to as PHI1A and PHI2A. The PHI1A and PHI2A signals are controlled by the control signals PGM and PGMV. When both PGM and PGMV are low, both PHI1A and PHI2A are pulled up to logic high (e.g., V_{CC}). When PGMV is high and PGM is low, PHI1A is

pulled up to V_{CC} while PHI2A is grounded. Finally, when PGMV is low and PGM is high, PHI1A is logically equivalent to PHI1 while PHI2A is equivalent to PHI2. In other words, when PGM is high and PGMV is low, PHI1A and PHI2A function as a pair of non-overlapping two phase clock signals. It should be noted that, by design, there will never be a situation whereby both PGM and PGMV are both high. Circuit block 105 comprises a voltage level shifter that converts the control signal ENVPP to a level shifted inverted signal, VPPONBH.